

PLL IP cell

Main characteristics

- Silterra 130 G
- 1.2V \pm 10% power supply
- -40 to +125°C

Deliverables

- GDS II layouts
- LEF abstracts
- CDL netlists
- Liberty timings
- Verilog description
- A full datasheet
- An integration note

Status

- Silicon proven

Product description

The nSOSC_SIL130G_1V2 PLL2G cell is a fully-programmable PLL IP cell powered at 1.2V \pm 10% designed on the Silterra 130 G technology. Its input reference frequency can be chosen between 1 and 250MHz and the output between 62.5MHz and 2GHz.

Applications

- Clock multiplication
- Clock recovery
- High-speed generator for Ser/Des PHYs

Main features

- Type II, 3rd order low jitter PLL
- Single 1.2V \pm 10% power supply
- 62.5MHz – 2GHz programmable output frequency (D = 1-16)
- Programmable serialization factor (N = 1-10)
- Programmable charge-pump frequency (P = 1-16)
- PLL jitter spectrum optimization
- -40 to +125°C junction temperature
- Standby/power down mode
- Low silicon surface



Further information

For further information about this product and other nSilitation IPs, development roadmap, availability and licensing terms, please e-mail to sales@nsilitation.com.

Delivery and support

This reference voltage cell is available as hard macro-cell for reuse in any design based on the Silterra 130 G CMOS process. No extra IP license from any third party will be needed for the cells or the cell library.

In addition, full support service is available on request. Support can include close integration follow-up by our design team or custom-made cells or features.

Porting to another process

The nSOSC_SIL130G_1V2 PLL2G IP cell is silicon proven in the Silterra 130 G CMOS process. It can be easily ported to another foundry and/or another similar CMOS process node upon request. Please contact us for details and availability.

About nSilitation

nSilitation is a leading analog and mixed-signal semiconductor IP provider.

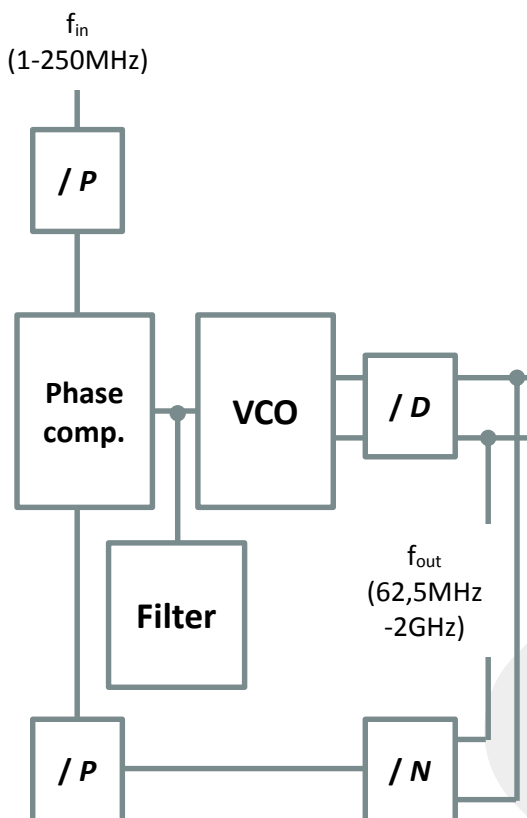
nSilitation specializes in the development of high quality analog and mixed-signal high performance semiconductor IPs. With reference designs available for 10b to 14b A/D and D/A converters, high-speed IO circuits, PFM and PWM high efficiency DC/DC integrated converters and high precision bandgap references; nSilitation enables the highest value analog and mixed-signal functionalities at the lowest risk.

The "IP design" service of nSilitation offers top-class quality, customization and support dedicated to your needs and your specifications.

Disclaimer

The information provided by nSilitation has been verified and is believed to be accurate. nSilitation and all its right holders reserve the right to make changes to the information contained herein without notice. They reserve also the right to make changes to the product without notification. No liability shall be incurred as a result of the use or application of the information provided in this data sheet and/or the use of the corresponding product in any case.

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Phase locked loop block diagram

